CLAIMS:

1. Linear phase detector comprising at least a first circuit (1) receiving at least one first clock signal (CLK00) for generating at least one first control signal (UP,U1) and at least a second circuit (2) receiving at least one second clock signal (CLK90) for generating at least one second control signal (DOWN,U2), wherein each one of said circuits (1,2) comprises at least two latches (10,11,20,21) and at least one multiplexer (12,22) for multiplexing latch output signals.

2. Linear phase detector according to claim 1, wherein first latches (10,11) of said first circuit (1) receive at least one data signal (DATA), with a first multiplexer (12) of said first circuit (1) generating at least one first multiplexer output signal destined for second latches (20,21) of said second circuit (2).

3. Linear phase detector according to claim 2, wherein first logical circuitry (13) of said first circuit (1) receives said data signal (DATA) and said first multiplexer output signal for generating said first control signal (UP,U1), with second logical circuitry (23) of said second circuit (2) receiving said first multiplexer output signal and at least one second multiplexer output signal for generating said second control signal (DOWN,U2).

4. Linear phase detector according to claim 1, wherein said linear phase detector comprises at least a third circuit (3) receiving said first clock signal (CLK00) for generating at least one third control signal (U3) and at least a fourth circuit (4) receiving said second clock signal (CLK90) for generating at least one fourth control signal (U4), wherein each one of said circuits (3,4) comprises at least two latches and at least one multiplexer for multiplexing latch output signals.

5. Linear phase detector according to claim 4, wherein third latches of said third circuit (3) receive at least one second circuit output signal, with a third multiplexer of said third circuit (3) generating at least one third multiplexer output signal destined for fourth latches of said fourth circuit (4).

6. Linear phase detector according to claim 5, wherein third logical circuitry of said third circuit (3) receives said second circuit output signal and said third multiplexer output signal for generating said third control signal (U3), with fourth logical circuitry of said fourth circuit (4) receiving said third multiplexer output signal and at least one fourth multiplexer output signal.

7. Linear phase detector according to claim 6, wherein each one of said logical circuitry is coupled to an adder/subtracter (5).

8. Clock extractor and data regenerator comprising a linear phase detector with at least a first circuit (1) receiving at least one first clock signal (CLK00) for generating at least one first control signal (UP,U1) and at least a second circuit (2) receiving at least one second clock signal (CLK90) for generating at least one second control signal (DOWN,U2), wherein each one of said circuits (1,2) comprises at least two latches (10,11,20,21) and at least one multiplexer (12,22) for multiplexing latch output signals.

9. Method for linearly phase detecting and comprising a first step of receiving at least one first clock signal (CLK00) for generating at least one first control signal (UP,U1) and a second step of receiving at least one second clock signal (CLK90) for generating at least one second control signal (DOWN,U2), wherein said steps each comprise the substeps of latching and of multiplexing results from said latching.

10. Processor program product for linearly phase detecting and comprising a first function of receiving at least one first clock signal (CLK00) for generating at least one first control signal (UP,U1) and a second function of receiving at least one second clock signal (CLK90) for generating at least one second control signal (DOWN,U2), wherein said functions each comprise the subfunctions of latching and of multiplexing results from said latching.

11. Apparatus comprising a clock extractor and data regenerator comprising a linear phase detector with at least a first circuit (1) receiving at least one first clock signal (CLK00) for generating at least one first control signal (UP,U1) and at least a second circuit (2) receiving at least one second clock signal (CLK90) for generating at least one second

control signal (DOWN,U2), wherein each one of said circuits (1,2) comprises at least two latches (10,11,20,21) and at least one multiplexer (12,22) for multiplexing latch output signals.